

REMARKS

This paper is responsive to the Office Action dated May 5, 2004. Claims 1, 2 and 5 - 7 are pending in this application and have been rejected. Reexamination is respectfully requested in light of the following remarks and attached declaration.

Claim Rejections - 35 USC § 112

Claims 1 - 2 and 5 - 7 have been rejected under 35 USC § 112 (second paragraph) as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant respectfully traverses this rejection for the reasons that follow.

As the Examiner has recognized, Applicant claims this invention using certain product by process limitations. These process limitations are clearly limited to the product. The product is a Known Good Die (KGD). Known Good Dies are in themselves a product, and are quite different from dies which are manufactured without additional testing, such as stress-tolerance testing which may include thermal-stress testing (Applicant's specification, page 6, at the bottom, and page 7). The thermal-stress test is a component of Applicant's Known Good Die test, which is necessary to define the Known Good Die. Known Good Dies are defined as equivalent quality and reliability of the

comparable package part (see attached article, "KGD: A State of the Art Report" by Jim Rates.

Applicant claims structure and a process of manufacture which produces the claimed Known Good Die (KGD).

The Examiner asks what structure necessarily results from this process limitation. The answer is a Known Good Die that has been tested for thermal stress tolerance and, therefore, has been screened to eliminate dies that do not possess it (see attached Danziger Declaration).

The Examiner argues that the process limitation bears insignificant patentable weight for the product since a person has no way to structurally discern that something was stress tolerance tested prior to mounting. As the Danziger Declaration shows, Known Good Die testing, such as stress tolerance testing, is specified by the user of the die. This is especially important for certain end uses such as multichip modules, and satellite application (Danziger Declaration). Therefore, the consumer who has specified the required Known Good Die, certainly knows what he has specified and what is contained in its design manufacture and ultimate statistical probability of being a Known Good Die.

Next, the testing prior to mounting of Applicant's claimed die is also very apparent from visual examination of the claimed KGD. If the connections are made to the solder ball connections, the solder balls will be imperfect and will shown signs of prior connection, such as a taffy pull configuration. This type of

connection reveals prior use and the unavailability for future use. Similarly, prior use of wire bond connections can be easily determined by visual inspection (a microscope may be necessarily). The disruption of the wire bond connections allows a person to structurally discern that there has been testing on them. The fact that the dies have been specified for thermal stress tolerance (Known Good Dies) combined with physical evidence of testing is complete proof.

35 USC § 287 makes it incumbent upon the patent owner to provide constructive or actual notice to the infringer in order to collect any damages at all. Therefore, the infringer will be notified by the patentee. It is the patentee's duty to find the infringer. Next, as a matter of trial procedure, it is the patentee's burden of proof to prove infringement under 35 USC § 271. It is the patentee who must muster the facts of infringement against a potential infringer. Still further, the "potential infringer" if he manufactures the claimed known good die and device together will certainly know the process used to make the Known Good Die. On the other hand, should the "potential infringer" purchase his dies, he will certainly have the ability to find out if his device contains dies which have or have not been tested.

In fact, he will have specified the thermal stress tested KGD (Danziger declaration). The "potential infringer" is a hypothetical person who has no standard for determination.

Applicant cannot respond to such an allegation because the Examiner has presented no evidence as to the level of skill of a potential infringer.

Next, at page 2, line 19 the Examiner refers to scope of structure. The file history of this application provides an answer. Therefore, there must be a structural difference (see MPEP § 2113). Such a structural difference was previously outlined to the Examiner in Applicant's paper filed September 10, 2003 in discussion of the rejection under 35 USC § 102. The "potential infringer" need only refer to this to determine one of the differences which have apparently been recognized by this Examiner in dropping the rejection under 35 USC § 102.

The clear test for product by process claim patentability is prior art, not some potential future infringement. Claims are not unpatentable because of a potential future infringer. Instead, claims once patented provide the basis for actions against future potential infringers.

At page 2, lines 20 - 24, the Examiner first notes that how the device was tested to describe the structure is part of its history. Next, the Examiner states, "so what one must ask is: what happens to a structure that was 'thermal stress tested'?" The answer is taught in Applicant's specification that the thermal test tolerance screening is used to eliminate dies which

do not pass the test. Stated another way, dies that fail the test never appear in an end use device in the first place (they are not KGD). This is one indicia of what happens. Next, the Examiner asks, "What does it look like ...?" The answer is that it works when others do not. Stated more simply, the device that does not pass the thermal stress test becomes broken and it never appears as a Known Good Die in the first place. Two computers can "look" alike, but the programming or chip structure may differ. The test for infringement in the computer example is if the software or hardware responds to claims of a patent.

At page 2, beginning at line 5 up from the bottom, the Examiner asserts:

"In claim 1, the last six lines are directed to how the earlier recited 'solder ball array connections' and 'wire bond connections' are 'used' and 'connected' and 'not connected' at various points during a process. The acts do not give rise to a discernable structure in the finally claimed product: what do the 'wire bond connections' and solder ball array connections physically look like in the product?"

The answer to this question is found in simple observation the Known Good Die in accordance with claim 1. Either the solder ball array connections or the wire bond connections will have been disturbed and will no longer be pristine (see discussion of pristine *infra*).

This is discernable by optical inspection of the die and the availability of connections for use in an end use device is apparent. Applicant respectfully refers the Examiner to US Patent 5,886,414 (relied upon in this Office Action). At column 5, lines 17 to 23 where that patent also teaches that "since the previous testing connections were made to the extension areas, there remains an undamaged region to make electrical connections for final packaging." Applicant respectfully submits that the '414 use of the term "undamaged areas available for electrical connections" is no different than Applicant's reference to used or not used in claim 1 or the more precise definition of undamaged as found in claim 2, where Applicant refers to connections remaining pristine and until connected to the end use device. "Pristine" in Applicant's specification (Applicant is entitled to be his own lexicographer) has the same meaning as an undamaged region as found in the '414 Galloway patent at column 5, lines 17 - 21. It merely means undamaged. The Examiner is respectfully requested to refer to Applicant's specification at page 3, lines 8 - 12, page 5, lines 13 - 16, page 10, lines 19 - 25, page 11, last line - page 12, line 6, Applicant's original claim 12, original claim 21, original claim 34, and original claim 42. It is clear from the above references in Applicant's specification that Applicant has elected to use the word "pristine" as meaning that the reference connections are not used. Pristine clearly means undamaged and

available for connection in an end use device, such as an MCM (multichip module) or other device where a KGD must be specified.

The Examiner asks if connections remain pristine in time, what do they look like in the product compared to prior art connections that are not pristine. The answer is explained in the specification, which is that they are unused. What they look like is that they are not damaged or, as stated in the language of '414, remain undamaged to make electrical connections for final packaging.

The limitation in claim 5 stating that connections are not removed from the die first provides definition over the breakaway disclosure in US Patent 5,886,414, Galloway, which is relied upon as prior art in the rejection under 35 USC § 103. Applicant leaves the connections on the die (does not remove them) although they are damaged after the test. Claim 1 simply does not implicitly recite a device having connections that are removed. Claim 1 recites alternate use of wire bond connections or solder ball connections for a known good die test. Claim 1 does not state that these connections are removed from the die. Claim 1 states that there are solder ball array connections on the planar KGD surface and wire bond connections on the planar KGD surface. These are the connections that are not removed. Claim 1 simply does not refer to removal of these connections or any other connections. Stated another way, claim 1 does not recite a step

of how or when contacts between the connections and a test device are removed.

The Examiner at page 3 has stated:

For purposes of examination, the "solder ball connections" and "wire ball connections" of the claimed product are any discernable electrical contact structures that are or were "solder ball connections" or "wire bond connections," respectively.

This observation by the Examiner is respectfully traversed. Claim 1 recites that the KGD at all times has solder ball array connections on the planar KGD surface and at all times has wire bond connections on the planar KGD surface. Claim 1 does not respond to the language as interpreted by the Examiner.

Claim Rejections - 35 USC § 103

The Examiner has rejected claims 1 - 2 and 5 - 7 as being unpatentable over Galloway '414 in view of IEEE 1995 taken with flip chip reference Sherif '394.

The Examiner has cited Shaukatullah and Sherif to conclude that it would be obvious to modify the metal bumps (24) of Galloway to include solder balls. Applicant respectfully requests that the Examiner refer to Applicant's specification, page 5, top five lines, which refer to flip chip technology and C4 technology. These technologies Applicant acknowledges include solder balls. Still further, the '414 reference at column 3, beginning at line



29, states that the metal bump (24) allows the die to be used in a flip chip or tape-automated-bonding (TAB) package. Applicant, therefore, concludes that in view of the '414 teaching and Applicant's teaching that Applicant's claims for solder ball array connections apply to flip chip and C4 technology as well. Since this is Applicant's position, there is no need to go beyond '414 in considering patentability of Applicant's claims.

Applicant also equates the terminology solder ball or flip-chip C4 array at Applicant's specification, page 9, lines 14 - 17.

Galloway '414

Galloway discloses a chip with extension layers of a metal layer extending over a passivation layer. These extension layers are for connections by use of wire bond pads to allow an electrical connection with the original wire bond pads for burn in testing. The testing connections, (extension areas) can be removed without damaging regions on the die for the final packaging connections.

In Applicant's claim 1, Applicant requires that the claimed KGD have both solder ball array connections and wire bond connections on the planar KGD surface. This structure is shown in Applicant's Figures 1, 2 and 3 where the solder ball connections (10) and the wire bond connections (12) are on a single planar surface of the die (14). Similar structure is shown in Figures 1

and 1B. The die has connections between all of the solder ball array connections and wire bond connections. The definition of the word "planar" is that of a plane or a surface having a flat 2-dimensional quality. In '414, neither the bumps (24), nor the wire bond connectors (12a) (see Figure 1) are mounted on a planar KGD surface. Instead, they are above the planar KGD surface. The only on the planar surface of the die (14) in '414 is a wire bond pad made of aluminum (16). Everything else, such as the extension area (12a) and metal bumps (24) are stacked on top of the wire bond pad (16). For this reason, '414 simply does not anticipate or render obvious the first two clauses of claim 1.

Applicant, therefore, traverses the Examiner's observation that the "KGD having solder bump array connections on a planar KGD surface (e.g., bumps 24 are "on" and "over" the upper planar surface of the KGD 14)". Review of Figure 1 and the other figures of the '414 patent, shows that neither the bumps nor the wire bond connections are on the KGD planar surface as claimed.

Next, the Examiner has argued that bumps (24) are "on" and "over" the upper planar surface of KGD (14). Applicant's claims require not only that the solder ball array connections be on the planar surface, but also that the wire bond connections be on the planar KGD surface. This is simply not the case with '414 when neither is on the planar KGD surface, and where the bumps (24) are on a surface of material (12), which is part of material (12a), which is placement of the bump (24) on a portion of the bond area.

Still further, a view as shown in Figure 1 shows that both bumps (24) and pads (12a) are placed upon a single wire bond pad (16), which is in turn placed on the dye (14). The only thing on dye (14) is wire bond pad (16). The Examiner is requested to refer to the definitions of "on" and "over" which are attached to this amendment. These definitions are consistent with Applicant's argument, and show that the two terms do not mean the same thing.

Next, the Examiner asserts that '414 teaches a thermal stress test. Review of '414 first shows that it relates to burn in testing, not a thermal stress test. On the other hand, '414 in its design shows that it does not take thermal stress testing into consideration. First, as pointed out in Applicant's specification, thermal stress testing requires a particular lay out of the ball-grid array on the face of the planar surface in order to allow and compensate for the thermal stress. Here, the bumps are not even on the planar surface, and there is no teaching that the bumps are designed and laid out to accommodate thermal stress. However, and more importantly, the extension areas are described as being weak and brittle (see column 4, lines 55 - 60).

With this design, it becomes very clear that '414 not only does not suggest thermal stress testing, it teaches away from such thermal stress testing by utilizing weak and brittle extension areas (12a). In '414, the flow chart depicted in Figure 9 shows only a burn in testing and does not suggest a thermal stress test as claimed by Applicant.

The Examiner asserts that in the alternative solder ball connections are used and refers to step (84) of Figure 9. The alternative referred to is the use of solder ball connections to a test device. However, step (84) of Figure 9 relates to the burn in testing. This step follows connecting to extension areas with wire bonds (step 82b) connecting to extension areas (82c) or touching with probes. Figure 9 simply does not disclose use of the bumps (24) as the alternative connections to be used during a thermal stress test tolerance test as claimed. Throughout '414, there is no suggestion that the bumps (24) are ever used for any purpose other than the end use. The extension areas (12a) are always used for test, and the extension areas (12a) are the ones that may be broken off or removed after test. There is no alternative of either wire bond connections or solder ball connection used for Known Good Die tests disclosed by or suggested by '414.

The Examiner should note that column 5, lines 15 - 24 teaches that the Known Good Dies can be packaged making connections to locations other than the extension areas in step (88). It further states that the packaging can be done with connections to the metal bumps. Still further, it states that since previous connections were made to extension areas, there remains an undamaged to make electrical connections for the final packaging.

This does not suggest alternative use of the bumps for testing. In step (90) shown in Figure 9, the step is providing the Known

Good Die to the customer. The Known Good Die provided to the customer is one created by the previous steps (80) through (86). This Known Good Die, however, is not one, which is proven to be a Known Good Die by making connections to the bumps or ball contacts.

#### Claim 2

Claim 2 recites that if solder ball connections, the wire bond connections remain pristine. Galloway teaches only the opposite.

#### Claim 5

Claim 5 clearly defines over Galloway in that claim 5 teaches that the bond connections are not removed from the planar surface. On the other hand, step (86) while reciting "optionally removing extension areas," fails to place the pads on the planar surface of the Known Good Die in the first instance. As pointed out above, the extension areas (12a) are simply not on the die planar surface. Even though they may not be removed, they are simply not on the planar surface of the die to begin with.


#### Summary

It is, therefore, respectfully submitted that the '414 reference does not meet the term of the claims or reasonably

suggest to one skilled in the art the structural limitations of the claims or the process limitations of the claims.

In view of the foregoing, it is respectfully submitted that the application is now in condition for allowance, and early action in accordance thereof is requested. In the event there is any reason why the application cannot be allowed in this current condition, it is respectfully requested that the Examiner contact the undersigned at the number listed below to resolve any problems by Interview or Examiner's Amendment.

Respectfully submitted,



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Date: July 2, 2004

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# KGD

## A STATE OF THE ART

## REPORT

With processes and techniques constantly changing, the need for low FIT rate bare die is real. BY JIM RATES

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**T**he term known good die (KGD) has been with us for almost 10 years. Many techniques for making an electrical interconnect to the die bond pads, in order to facilitate test and burn-in, have come and gone. But a few still remain. Over the years the description of KGD has changed little. The "equivalent quality and reliability of the comparable packaged part" is still valid. The description of failure rates is changing from the old "3 to 9s" or "4 to 9s" to failures in time or FIT rate. And the different applications and assembly processes can tolerate different FIT rates. Additionally, some wafer fab processes lend themselves to other than carrier KGD processing techniques. One of the new (old) techniques involves some unique test conditions accompanied by electrical stress that can accelerate defects that can be detected using Iddq testing. This article addresses the new techniques, the state of surviving carrier techniques and user needs.

### Background

Quality and reliability are separate qualities. However, if FITs are screened out to an acceptable level, by definition the initial quality should be 100 percent. Therefore, today's discussions about KGD center on FIT rates.

In 1996, I published an article<sup>1</sup> chronicling the past, present and future of

KGD. In my conclusions I stated that "The future is bright for KGD. They just will not be called KGD." This has been borne out by the proliferation of single die chip scale packages (CSP) that have become available in the last few years. This availability of CSPs provides solutions for at least two of the problems associated with KGD, while in some cases providing a die size packaging solution. The first is the elimination of handling problems associated with KGD. Automatic handlers can be used for test, burn-in and assembly without fear of damaging the die. Secondly, automatic handlers can provide a simple common interface for electrical connection.

There are a number of sockets available today, down to 0.5 mm pitches, that make reliable connections to CSPs. Loranger, Wells-CTI and Yamaichi make sockets that work well on small pitch BGAs, but they may or may not work on flip chip bumped die or CSPs that resemble flip chips. Those technologies should not be confused with Aehr Test, Bear Technology, or Texas Instruments (TI)/Micro Modules Systems (MMS) sockets that are intended for bare die, bumped or unbumped. Yamaichi does offer sockets for both small pitch BGAs, flip chip and tape-automated bonding (TAB).

Several reports are available today listing current and past die/KGD usage, as well as predictions for future use. These

reports infer that millions (sometimes billions) of die are presently being used and the trend is upward. It is difficult to separate the uses/users and the areas of the world involved, but the major users of bare die today are still the semiconductor manufacturers. If the manufacturers package two or more die into a package, they become a die usage statistic. A large number of TAB die are used in Asia, further skewing the numbers.

James B. Brinton published an article<sup>2</sup> discussing the fading multichip module (MCM) market growth. The article states that according to an upcoming report from Prismark Partners LLC, 275 million KGD were shipped in 1997 compared to 4.2 billion in total bare die shipments, and 53.3 billion total integrated circuit (IC) die in all forms. The article further defines KGD as die "tested beyond conventional wafer probe." These numbers are mind boggling. As an employee of the premiere die processor in the industry, I can state without fear of contradiction that Chip Supply Inc. (CSI) and all of its competitors did not ship the noted bare die or KGD in 1997. In fact those numbers have not been reached in the combined lifetime of the companies. I can further state that all of the companies supplying KGD carriers, sockets, burn-in boards and assorted other widgets did not and cannot support this KGD run rate.

So where did they come from and where did they go? I don't know! But I do have some thoughts. Tested beyond conventional wafer probe does leave room in defining KGD. As mentioned earlier, different applications can tolerate different quality levels and FITs. Simply adding a special parameter at probe such as Taa or Iddq could make the die "good enough." This area accounts for a large percentage of the delivered/consumed KGD by semiconductor manufacturers.

IBM is and has been producing C4 KGD (IBM fab) for years originally using their R3 KGD process, and more recently advanced applications of Iddq screening. Likewise, Delco has been producing flip chip KGD of their own manufacturer for years. These two companies alone contribute largely to the total. Contract assemblers such as Celestica and SCI also use large quantities of bare die mostly procured directly from the manufacturers.

Samsung and TI, among others, have been producing high volumes of fully screened single die chip scale packaged parts for several years. These must be in the count as well as the Asian captive market.

We are not alone in trying to understand the "state of the art of KGD." Remy Degen authored an article titled "KGD: Konfusing Signals,"<sup>3</sup> which amply describes the technical state of KGD today. He evaluates the feasibility of KGD by reviewing the standard process minus the assembly step; he points out the biggest obstacle is burn-in, which is not necessary on some products; and he discusses the possible use of wafer level burn-in as a solution to volume KGD processing.

The quality and reliability exhibited

by any single semiconductor die is attributable to manufacturing defects caused during and by the wafer fab process. Defects such as weak oxides, bridging faults due to resistive via contacts, certain open faults, stuck-on faults, operation induced faults, parasitic devices, pn junction leakage and abnormally high contact resistance all contribute to the quality and reliability of any single die. Many of these defects may not manifest themselves as normal logic fault failures, and therefore, may not be detected by traditional logic functional testing. Many of these faults are activated using current burn-in screening techniques.

Today, there are ongoing studies to model and demonstrate wafer level die processing techniques that allow the screening of bare die that meet military requirements for packaged parts without burn-in or the use of special carriers.

#### Surviving Carrier Technologies

In order to screen bare die in the same manner as packaged parts, a method must be used to make a reliable electrical connection to the die bond pads. This is not trivial because the bond pads most likely will have a layer of native oxide on them. The interconnect method must penetrate this barrier and make a low impedance contact to the aluminum. Over the last 10 years many techniques have surfaced to accomplish this, but only four have survived. These four have been used, and in some cases, are still being used to screen bare die. Following is a status report on these four technologies:

- 1) SoftTAB is a patented process used by CSI to produce KGD. The process is described in U.S. patent 5,677,203. To date the company has not offered licensing of SoftTAB, but continues to use the process to supply KGD.
- 2) Bear Technologies was a joint venture between Micron Semiconductor and Cybex Corp. The carrier offered made use of the highly effective silicon interconnect technology developed

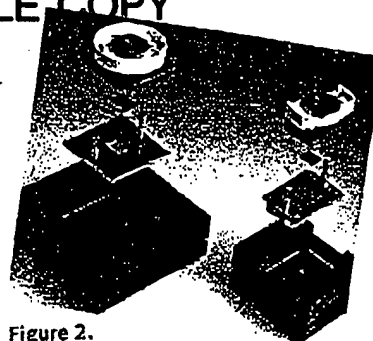


Figure 2.  
The DieMate product line,  
developed by Micro Modules  
Systems.

by Micron's advanced packaging group known as KGD Plus (Figures 1 and 1a). Several patents issued to Micron protect this process. The complete carrier (package and insert) were manufactured by Micron, and the assembly/disassembly equip-

ment was manufactured by Cybex. This arrangement allowed Bear to offer the only turnkey system available for producing KGD.

Several months ago, Cybex filed for protection of the bankruptcy court. Cybex was liquidated and the remaining assets were sold. Micron, as the remaining majority partner, made the decision to shut down Bear. However, Micron intends to bring this product back to market.

3) TI/MMS — The DieMate (Figure 2) product line was originally developed by MMS and made use of a patented diamond particle interconnect system. TI and MMS entered an agreement that made TI the sales and marketing arm for DieMate. Over the years this interconnect system has evolved to the product currently offered by TI. MMS fabricates the insert and TI fabricates the carrier and performs the assembly.

However, recent news confirms that MMS is undergoing a re-financing process which may lead to a change in ownership or termination of some of the product lines. The impact of this on the DieMate product from Texas Instruments is being evaluated. James Forster<sup>4</sup>, DieMate product manager, has indicated that TI is committed to the DieMate product line and is working on developing alternate sources for the substrate.

4) Aehr Test Systems offers their line of DiePak components for KGD processing (Figure 3). This includes a temporary reusable die carrier, an interconnect substrate and a burn-in socket. The interconnect substrate consists of a proprietary polyimide film with fine line pitch copper traces and through holes filled with metal.



Figures 1 and 1a.  
The complete carrier  
(package and insert)  
developed by Micron's  
KGD Plus.



drugs) **b** — used as a function word to indicate involvement with the activity, work, or function of (the jury) (the duty) **c** — used as a function word to indicate position or status in proper relationship with a standard or objective (the schedule) **7 a** — used as a function word to indicate reason, ground, or basis (as for an action, opinion, or computation) (I have it ~ good authority) (the one condition) (the interest will be 10 cents ~ the dollar) **b** — used as a function word to indicate the cause or source (profited ~ the sale of stock) (the win came ~ a last-second goal) **c** — used as a function word to indicate the focus of obligation or responsibility (drinks are ~ the house) (put the blame ~ my actions) **8 a** — used as a function word to indicate the object of collision, opposition, or hostile action (bumped my head ~ a limb) (an attack ~ religion) (pulled a gun ~ me) **b** — used as a function word to indicate the object with respect to some disadvantage, handicap, or detriment (has three inches in height ~ me) (a 3-game lead ~ the second-place team) (the joke's ~ me) (it's no use denying it, we've got the goods ~ you) **9 a** — used as a function word to indicate destination or the focus of some action, movement, or directed effort (crept up ~ him) (feast your eyes ~ this) (working ~ my skiing) (made a payment ~ the loan) **b** — used as a function word to indicate the focus of feelings, determination, or will (have pity ~ me) (keen ~ sports) (a curse ~ you) **c** — used as a function word to indicate the subject of study, discussion, or consideration (a book ~ insects) (reflect ~ that a moment) (agree ~ price) **10** — used as a function word to indicate reduplication or succession in a series (loss ~ loss)

**on** \ˈɒn, ˈæn/ *adv* (bef. 12c) **1 a** : in or into a position of contact with an upper surface *esp.* so as to be positioned for use or operation (put the plates ~) **b** : in or into a position of being attached to or covering a surface; *esp.* in or into the condition of being worn (put his new shoes ~) **2 a** : forward in space or time (went ~ home) **b** : in continuance or succession (rambled ~) (and so ~) **3** : into operation, or a position permitting operation (switched the light ~)

**on** \ˈɒn, ˈæn/ *adj* (1541) **1** : engaged in an activity or function (as a dramatic role) **2 a** (1) : being in operation (the radio is ~) (2) : placed so as to permit operation (the switch is ~) **b** : taking place (the game is ~) **3** : INTENDED, PLANNED (has nothing ~ for tonight)

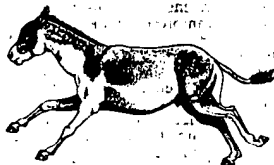
**on** \ˈɒn, ˈæn/ *n* *suffix* [ISV, alter. of -one] : chemical compound not a ketone or other oxo compound (parathion)

**on** \ˈɒn, ˈæn/ *n* *suffix* [fr. -on (in ion)] **1** : subatomic particle (neutron) **2 a** : unit : quantum (photon) (magneton) **b** : basic hereditary component (cistron) (operon)

**on** \ˈɒn, ˈæn/ *n* *suffix* [NL, fr. -on (in argon)] : noble gas (radon)

**on-again, off-again** *adj* (1948) : existing briefly and then disappearing in an intermittent unpredictable way (on-again, off-again fads)

**on-a-ger** \ˈɒn-ə-ˈdʒər/ *n* [ME, wild ass, fr. L, fr. Gk *onagros*, fr. *onos* ass + *agros* field — more at ACRE] (14c) **1** : a small pale-colored kiang with a broad dorsal stripe **2** [LL, fr. L] : a heavy catapult used in ancient and medieval times



onager 1

**on and off** (1855) : OFF AND ON

**onan-ism** \ˈɒn-ə-ˈnɪz-əm/ *n* [prob. fr. NL *onanismus*, fr. *Onan*, son of Judah whose disobedient act is described in Gen 38:9] (ca. 1727) **1** : MASTURBATION **2** : COITUS INTERRUPTUS **3** : SELF-GRATIFICATION — **onan-is-tic** \ˈɒn-ə-ˈnɪs-tɪk/ *adj*

**once** \wɒn(t)s/ *adv* [ME *ones*, fr. gen. of *on* one] (12c) **1** : one time and no more **2** : at any one time : under any circumstances : EVER **3** : at some indefinite time in the past : FORMERLY **4** : by one degree of relationship

**once** *n* (13c) : one single time : one time at least — **at once** **1** : at the same time : SIMULTANEOUSLY **2** : IMMEDIATELY **3** : BOTH

**once** *adj* (1691) : that once was : FORMER

**once-over** (1761) : at the moment when : AS SOON AS

**once-over** \wɒn(t)-sɔ-vər/ *n* (1914) : a swift examination or survey; *esp.* a swift comprehensive appraising glance

**once** *that conj* (1874) : ONCE

**oncho-cer-cla-sis** \ˈɒn-kə-ˈsɜr-ˈki-ə-səs/ *n*, *pl* -a-ses \-sɛz/ [NL, fr. *Onchocerca*, genus of worms] (1911) : infestation with or disease caused by filarial worms (genus *Onchocerca*); *esp.* a disease of man caused by a worm (*O. volvulus*) that is native to Africa but now present in parts of tropical America and is transmitted by several biting flies

**oncid-lum** \ˈɒn-sɪd-ə-ləm, ˈɒn-ˈkɪd-/ *n* [NL, fr. Gk *onkos* barbed hook — more at ANGLE] (ca. 1868) : any of a genus (*Oncidium*) of showy tropical American epiphytic or terrestrial orchids

**onco- comb form** [NL, fr. Gk *onkos* bulk, mass; akin to Gk *enenkein* to carry — more at ENOUGH] : tumor (oncology)

**onco-gen-e-sis** \ˈɒn-kə-ˈdʒen-ə-səs/ *n* [NL] (ca. 1932) : the induction or formation of tumors

**onco-gen-ic** \ˈɒn-ˈdʒen-ɪk/ *adj* (1936) **1** : relating to tumor formation **2** : tending to cause tumors

**onco-genic-ity** \ˈɒn-ˈdʒen-ɪ-ti/ *n* (1944) : the capacity to induce or form tumors

**onco-log-ist** \ˈɒn-ˈkɒl-ə-ˈdʒɪst, ˈɒn-/ *n* (1857) : the study of tumors — **onco-log-ic-al** \ˈɒn-kə-ˈlɒj-ɪ-kəl/ *also* **onco-log-ic** \-ɪk/ *adj* — **onco-log-ist** \ˈɒn-ˈkɒl-ə-ˈdʒɪst, ˈɒn-/ *n*

**on-com-ing** \ˈɒn-kəm-ɪŋ, ˈɒn-/ *adj* (1844) **1 a** : coming nearer in time or space (the ~ year) (an ~ car) **b** : FUTURE (looked forward to his ~ visit) **2** : EMERGENT, RISING (the ~ generation)

**on-cor-na-vi-rus** \ˈɒn-kə-ˈrɒ-nə-ˈvi-rəs/ *n* [onco- + RNA + virus] (1970) : any of a group of RNA-containing viruses that produce tumors

**one** \wɒn, wən/ *adj* [ME *on*, *an*, fr. OE *ān*; akin to OHG *ein* one, L *unus* (OL *oinos*), Skt *eka*] (bef. 12c) **1** : being a single unit or thing (day at a time) **2 a** : being one in particular (early ~ morning) **b** : being preeminently what is indicated (~ fine person) **3 a** : being the same in kind or quality (both of ~ species) **b** (1) : constituting a unified entity of two or more components (the combined elements form ~ substance) (2) : UNITED **4** : existing or occurring as something not definitely fixed or placed (will see you again ~ day) **5** : being the

only individual of an indicated or implied kind (the ~ person she wanted to marry) — **at one** : at harmony : in a state of agreement

**one** \wɒn/ *n* (bef. 12c) **1** — see NUMBER table **2** : the number denoting unity **3** : the first in a set or series; *esp.* an article of clothing of a size designated *one* (wears a ~) **4** : a single person or thing (has the ~ but needs the other) **5** : a one-dollar bill

**one** \wɒn, wən/ *pron* (13c) **1** : a certain indefinitely indicated person or thing (saw ~ of his friends) **2 a** : an individual of a vaguely indicated group : anyone at all (~ never knows) **b** — sometimes used as a third person substitute for a first person pronoun (I'd like to read more but ~ doesn't have the time)

*usage* Senses 2a and 2b are usu. signs of a formal style. A formal style excludes the participation of the reader or hearer; thus *one* is used where a less formal style might address the reader directly (for the consequences of such choices, *one* has only oneself to thank — Walker, Gibson). Use of *one* to replace a first-person pronoun — criticized by some commentators — appears to be more common in British English than American English. It may be resorted to in order to avoid repetition of *I* (I'm watching this pretty carefully and I hope that the issue will come up in the Lords and *one* may be able to speak about it — Donald Coggan, Archbishop of Canterbury)

**one** \ɒn/ *n* *suffix* [ISV, alter. of -ene] : ketone or related or analogous compound or class of compounds (lactone) (quinone)

**one another** *pron* (13c) : EACH OTHER *usage* see EACH OTHER

**one-armed bandit** \wɒn-ˈɑrmd/ *also* **one-arm bandit** *n* (1934) : SLOT MACHINE **2**

**one-bag-ger** \wɒn-ˈbæg-ər/ *n* (1952) : SINGLE **2**

**one-dimensional** \wɒn-ˈdɪmənʃl/ *adj* (1883) **1** : having one dimension **2** : lacking depth : SUPERFICIAL (~ stereotype characters) — **one-dimensionality** *n*

**one-egg** *adj* (1948) : MONOZYGOTIC

**one-fold** \wɒn-ˈfɒld, ˈfɒld/ *adj* [ME, fr. OE *ānfeald*, fr. *ān* one + *feald* -fold] (bef. 12c) : constituting a single undivided whole

**one-handed** \ˈhæn-dəd/ *adj* (15c) **1** : having or using only one hand (could beat him up ~) **2 a** : designed for or requiring the use of only one hand **b** : effected by the use of only one hand

**one-horse** *adj* (1750) **1** : drawn or operated by one horse **2** : of little real importance or consequence (a ~ town)

**Onei-da** \ˈɒ-ni-də/ *n*, *pl* *Oneida* or *Oneidas* [Iroquois *Onéyōde*, lit., standing rock] (1666) **1** : an American Indian people orig. of New York **2** : a member of this people **3** : the language of the Oneida people

**one-ric** \ˈɒ-ni-rik/ *adj* [Gk *oneiros* dream; akin to Arm *anur* dream] (1859) : of or relating to dreams : DREAMY — **one-ric-al-ly** \-nɪ-k(ə)-li/ *adv*

**one-ro-man-cy** \ˈɒ-ni-rə-mən(t)-sɛ/ *n* [Gk *oneiros* + E -mancy] (1652) : divination by means of dreams

**one-line octave** *n* (1931) : the musical octave that begins on middle C — see PITCH illustration

**one-liner** \wɒn-ˈli-nər/ *n* (1967) : a very succinct joke or witticism

**one-man** *adj* (1842) : of or relating to just one individual : **a** : consisting of only one individual (a ~ committee) **b** (1) : done, presented, or produced by only one individual (a ~ stage play) (2) : featuring the work of a single artist (as a painter) (a ~ show of oils) **c** : designed for or limited to one individual

**one-ness** \wɒn-nəs/ *n* (1594) : the quality or state or fact of being one : **a** : SINGLENES **b** : INTEGRITY, WHOLENESS **c** : HARMONY **d** : SAME-NESS, IDENTITY **e** : UNITY, UNION

**one-night-er** \wɒn-ˈni-t-ər/ *n* (ca. 1937) : ONE-NIGHT STAND

**one-night stand** *n* (1880) **1** : a performance (as of a play or concert) given (as by a traveling group of actors or musicians) only once in each of a series of localities **2 a** : a locality used for one-night stands **b** : a stopover for a one-night stand **3** : a sexual encounter limited to a single occasion

**one-off** \wɒn-ɒf/ *adj*, *Brit* (1934) : limited to a single time, occasion, or instance : ONE-SHOT — **one-off** *n*

**one-on-one** \wɒn-ɒn-ˈwɒn, wɒn-ɒn-/ *adj* or *adv* (1967) **1** : playing directly against a single opposing player **2** : involving a direct encounter between one person and another

**one-piece** *adj* (1880) : consisting of or made in a single undivided piece (a ~ bathing suit) — **one-piece** \wɒn-ˈpiːs-/ *n*

**onerous** \ˈɒn-ə-rəs, ˈɒ-nə-/ *adj* [ME, fr. MF *onerous*, fr. L *oneratus*, fr. *oner-*, *onus* burden; akin to Skt *anas* cart] (14c) **1** : involving, imposing, or constituting a burden : TROUBLESOME (an ~ task) **2** : having legal obligations that outweigh the advantages (~ contract) — **onerously** *adv* — **onerous-ness** *n*

*syn* ONEROUS, BURDENSOME, OPPRESSIVE, EXACTING mean imposing hardship. ONEROUS stresses being laborious and heavy *esp.* because distasteful; BURDENSOME suggests causing mental as well as physical strain; OPPRESSIVE implies extreme harshness or severity in what is imposed; EXACTING implies rigor or sternness rather than tyranny or injustice in the demands made or in the one demanding.

**one-self** \ˈwɒn-sɛlf, Southern *also* ˈsɛf/ *also* **one's self** \ˈwɒn-, wɒnz-/ *pron* (1621) **1** : a person's self : one's own self — used reflexively as object of a preposition or verb or for emphasis in various constructions **2** : one's normal, healthy, or sane condition or self — **be oneself** : to conduct oneself in a usual or fitting manner

**one-shot** \wɒn-ʃʌt/ *adj* (1927) **1** : that is complete or effective through being done or used or applied only once (there is no easy ~ answer to the problem) **2** : that is not followed by something else of the same kind (a ~ tax cut) — **one-shot** *n*

**one-sided** \wɒn-ˈsɪd-əd/ *adj* (1813) **1 a** (1) : having one side prominent or more developed (2) : having or occurring on one side only **b** : limited to one side : PARTIAL (a ~ interpretation) **2** : UNILATERAL (~ decision) — **one-sided-ly** *adv* — **one-sided-ness** *n*

**one-step** \wɒn-ˈsteɪp/ *n* (1911) **1** : a ballroom dance in ¾ time marked by quick walking steps backward and forward **2** : music used for the one-step — **one-step** *vi*

**one-tailed** \wɒn-ˈtæɪld/ *also* **one-tail** \-tāl/ *adj* (1947) : being a statistical test for which the critical region consists of all values of the test statistic greater than a given value or less than a given value but not both — compare TWO-TAILED

**one-time** \wɒn-ˈtɪm/ *adj* (1840) **1** : FORMER, SOMETIME (a ~ actor) **2** : occurring only once : ONE-SHOT

**ovate** /'6.vət/ *adj* (1775) 1: shaped like an egg. 2: having an outline like a longitudinal section of an egg with the basal end broader (~ leaves).

over- prefix 1: so as to exceed or surpass 2: EXCESSIVE 3: to an excessive degree



ʌ\ about ʔ\ kitten, F table ɔr\ further ʌ\ ash ā\ ace ʌ\ cot, cart  
 ʌu\ out ʃh\ chin ɛ\ bet ē\ easy ɡ\ go ɪ\ hit ɪ\ ice ʊ\ job  
 ɪ\ sing ɔ\ go ɔ\ law ɔi\ boy ʰh\ thin ʰh\ the ʊ\ loot ʊ\ foot  
 ʌ\ yet ʒh\ vision ʌ, k, ʰ, œ, œ̄, ʉ, œ̄, ʰ\ see Guide to Pronunciation

10

S/N: 09/832,884

DOCKET NO.: L/M-102-DIV

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Serial No.: 09/832,884

Confirmation No.: 2718

Divisional of 09/321,565

Applicant: Steve M. Danziger, et al.

Art Unit: 2829

Filed: April 12, 2001

Examiner: Evan T. Pert

Docket No: L/M-102-DIV

Customer No: 28892

For: Method and Apparatus for Evaluating a Known Good Die Using  
Both Wire Bond and Flip-Chip Interconnects

Declaration of Steven M. Danziger

My name is Steven M. Danziger.

I reside at 10100 Tasker Drive, Manassas, Virginia. I am employed by BAE Systems Information and Electronic Systems Integration, Inc.

I am an inventor in US Patent Application 09/832,884, which has a filing date of April 12, 2001.

In an Office Action dated May 6, 2004 the Examiner has made the following statement:

"For purposes of examination, this process limitation bears insignificant patentable weight for the product, since a person has no way to structurally discern that something was "stress tolerance tested prior to mounting."

In the industry, persons determine whether a device is a Known Good Die (KGD) because they are specified at the time of purchase. Known Good Die by definition means that the product purchased (KGD) is one that has been electrically/thermally stress tolerance tested prior to mounting.

The reason for specifying a Known Good Die is to eliminate from a population of dies those which are weak or which may fail at a later time. This is necessary in constructing devices that are known as multichip modules (MCM). For instance, if only one die in ten is bad, and a multichip module includes as many as ten dies, then the probability of the MCM being a bad MCM is approximately 50%. Since it is very expensive to assemble MCM's, and expensive to discard MCM's with costly dies that will never be

S/N: 09/832,884

DOCKET NO.: L/M-102-DIV

used, it becomes incumbent upon the user of a die to procure KGD dies for assembly into MCM units.

On the other hand, if a die is merely to be used in a simply application, such as a cell phone, there is no need for a Known Good Die. In such a case, Known Good Dies are never even specified because it is cheaper to discard the cell phone component rather than test for a Known Good Die in the first instance.

In the most extreme example, Known Good Dies are an absolute requirement for use in satellite applications. In satellite applications it is not a simple matter to repair a satellite. The satellite when it fails can amount to a failure measured in hundreds of millions of dollars. In these applications, Known Good Dies which are previously stress tolerance tested are an absolute requirement and always used.

#### Inspection

The Examiner has failed to note that inspection of the Known Good Die set forth in claim 1 will easily reveal that the die has been tested. The reason is that the die as claimed has two sets of contacts, (wire bond connections and solder ball array connections.). And that once the die is tested, the connections used for testing (either solder ball array or wire bond) will be visibly disturbed. For instance, a solder ball connection will form imperfections in the balls, such as a taffy pull appearance when the connections are removed. Similarly, wire bond connections that have been disconnected are easily viewed. Stated another way, the connections which are not used are undamaged connections and, therefore, remain an undamaged region to which electrical connections for the final packaging may be made.

At page 2, beginning at line 11, the Examiner states:  
"In claim 1, the limitation 'which is thermal stress tolerance tested prior to mounting. . . by a test device' is clearly directed to the process, but not the product. What structure necessarily results from this process limitation?"

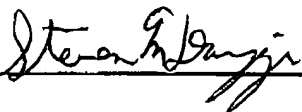
S/N: 09/832,884

DOCKET NO.: L/M-102-DIV

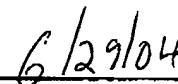
The answer is the claimed Known Good Die. Known Good Dies are a group of dies, which have been previously tested and screened to call out those that do not pass the screening test. This is a quality assurance procedure that produces a population of dies that are highly reliable and statistically far better than those which have never been tested. For instance, a group of dies wherein one die in ten is bad can be transformed into a Known Good Die group wherein only one die in one thousand is bad. Still further, the one die in one thousand would pass the screen, but then fail at a later point in time. Therefore, the product that is a Known Good Die is very different from a die that is not a Known Good die and which has not been tested. The structural difference is that the Known Good Die structure is one upon which confidence can be placed and which can be used with assurance in multichip modules and even in satellite applications. This is a significant product structural difference. The structural difference lies in the fact that the Known Good Die has a very, very low probability of failure.

I hereby declare upon penalty of perjury that the above statement is accurate and believed to be true. This statement is made with the knowledge that willful false statements and the like so made are punishable by fine and imprisonment, or both under Section 1001 of title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Signature: \_\_\_\_\_



Date: \_\_\_\_\_



Name: \_\_\_\_\_

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